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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/662,029 | 09/12/2003 | **Jyh Chain Lin** | | 9296 |

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| EXAMINER | |
|---|---|
| ALMO, KHAREEM E | |
| ART UNIT | PAPER NUMBER |
| 2816 | |

| MAIL DATE | DELIVERY MODE |
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| 08/11/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/662,029 | LIN, JYH CHAIN | |
| | Examiner | Art Unit | |
| | KHAREEM E. ALMO | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *7* is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's amendments filed 4/14/2008 have been received and entered in the case.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by AAPA.

With respect to claim 1, figures 4 and 6 of Applicant's admitted Prior Art discloses a pulse width modulation current adjustment apparatus comprising: a triangle wave generator (1) for generating a triangle wave voltage signal; a modulation voltage source configured for providing a modulation voltage signal (6) a comparator (2), a field effect transistor (3), a power supply (7), a first resistor (4), and a second resistor (5); wherein the triangle wave generator includes a first operational amplifier (leftmost Op Amp), a front resistor (not labeled but directly connected to ground), a first feedback resistor (R1), a second feedback resistor (R2), a first current limiting resistor (directly connected to D1 and the leftmost Op Amp), a second operational amplifier (Right most

Op amp with positive connection at uo), a second current limiting resistor (R3), a capacitor (C) and a back grounding resistor (R4); the front resistor electrically connects a negative terminal of the first operational amplifier to ground; the first feedback resistor, the second feedback resistor and the first current limiting resistor electrically connect to a positive terminal of the first operational amplifier so as to form a zero crossing comparator; the second operational amplifier, the second current limiting resistor, the capacitor and the back grounding resistor together form an integrator; the back grounding resistor electrically connects (via C R3 D2 and Uz) positive terminal (uo) of the second operational amplifier to ground; an output terminal of the first operational amplifier electrically connects to the positive terminal of the first operational amplifier via the first current limiting resistor and the first feedback resistor,; an output terminal of the second operational amplifier electrically connects to the negative terminal of the second terminal of the second operational amplifier via the capacitor; the output terminal of the second operational amplifier further electrically connects to the positive terminal of the first operational amplifier via the second feedback resistor; the output terminal of the second operational amplifier is configured for outputting the triangle wave signal the triangle wave voltage signal and the modulation signal are input to the comparator, an output of the comparator is connected to a gate terminal of the field effect transistor,, the first resistor is connected between the power supply (7) and a source terminals (S) of the field effect transistor, and a drain terminal (D) of the field effect transistor, outputs a pulse width modulation current signal driving current through the second resistor (5) to a load.

With respect to claim 2, figures 4 and 5 of AAPA disclose a pulse width modulation current adjustment apparatus as described in claim 1, wherein the triangle wave voltage signal is a symmetric triangle wave voltage signal (NOTE: the triangle wave voltage signal is a symmetric signal just not symmetric about the vertical axis; i.e. the individual triangles within each period form a perfect isosceles triangle with the base being the leftmost rising edge and the sides being the period at the right edge.)

With respect to claim 8, figure 6 of AAPA, discloses a triangle wave generator used in a pulse width modulation current adjustment apparatus , the triangle wave generator comprising a first operational amplifier (leftmost op amp); a front resistor (directly connected to ground) electrically connecting a negative terminal of the first operational amplifier (between R1 and D1 and ground); a first feedback resistor (R1) a second feedback resistor (R2) and a first current limiting resistor (connected to positive terminal of first operational amplifier at output) so as to form a zero-crossing comparator, a second operational amplifier (connected to uo) a second current limiting resistor (R3) and a capacitor (C) and a back grounding resistor (R4) together forming an integrator; the back grounding resistor (R4 grounded through Uz) electrically connecting a positive terminal of the second operational amplifier (directly connected to uo) to ground; and an output of the first operational amplifier (between R1 and D1) electrically connected to the positive terminal of the first operational amplifier via the first current limiting resistor (directly between D1 and 1$^{st}$ op amp) and the first feedback resistor (R1), an output of the second operational amplifier (connected to uo) electrically connected to the negative terminal of the second operational amplifier via the capacitor

(C) and also electrically connected to the positive terminal of the first operational amplifier via the second feedback transistor (R2), and the output of the second operation amplifier outputting a triangle wave voltage signal.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 4 of AAPA.

With respect to claims 3-6, figure 4 discloses a pulse width modulation current adjustment apparatus as described in claim 1, wherein the field effect transistor is a FET, but fails to disclose the details of the FET. It would be obvious to one skilled in the art at the time the invention was made to interchange different types of FET transistors for the purpose of optimizing the circuit to work in different environments. (i.e. to switch on a high signal, low signal etc.)

### *Response to Arguments*

6. With respect to applicant's argument AAPA fails to disclose or suggest that "the positive terminal of the second operational amplifier does not connect to anything", the Examiner disagrees. As shown in figure six there are 2 positive terminals of the operational amplifier. The back grounding resistor R4 electrically connects to the

positive terminal (uo) via intervening circuit (C) and connects the terminal to ground via D2 and Uz.

With respect to applicant's argument that AAPA fails to teach or suggest "the second operational amplifier, the second current limiting resistor, the capacitor and the back grounding resistor together form an integrator", the Examiner disagrees. The circuit forms an integrator because the capacitor is connected to the output of the second op amp and a resistor where vin is at the input of R3 and uo is the output are both functions of time.

With respect to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., new and unexpected results over AAPA and the functionality of the invention) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

With respect to applicant's argument that Has fails to teach or suggest the second operational amplifier and the back grounding resistor recited in claim 1, the Examiner agrees.

***Allowable Subject Matter***

7. Claims 9 and 10 are allowed.

8. With respect to claims 9 and 10, the prior art of record fails to disclose the circuit described in claim 1 wherein the triangle wave voltage signal consisting only of odd harmonics such that a percentage of the high frequency harmonics of the triangle wave voltage signal is low.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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1/9/2008

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PRIMARY EXAMINER
AU 2816

| Application Number | Application/Control No. | Applicant(s)/Patent under Reexamination | |
|---|---|---|---|
| | 10/662,029 | LIN, JYH CHAIN | |
| | Examiner | Art Unit | |
| | KHAREEM E. ALMO | 2816 | |